VIVEK Kumar

DoB: 30th of June 1998

★ Patna, Bihar, India

(+91) 916 2860 555 vivekkumarkausik@gmail.com LI linkedin.com/in/vk30/

Technical Skills

Technical skills: Verilog HDL, Python3, HTML5, CSS, C, Soldering, IoT

Tools: Xilinx Vivado, Ubuntu, Microsoft Office, Adobe Photoshop, Adobe Aftereffects

Languages: English (Upper Intermediate), Hindi (Native)

Experience/Internship

Maven Silicon Jan 2021 - Mar 2021

RTL Design Intern

Patna, Bihar

- Followed and enhanced the processes for smoothed operations under the guidance of the Project Manager.
- Explored the RTL design of the processor using Verilog HDL under Xilinx Vivado Ide.
- Explored ways to visualize and send a daily report of results to team members using Meetings (Zoom, GMeet).
- Completed the project RISC-V RV32I processor design under the guidance of the technical Instructor.

Experts hub Dec 2017 – Jan 2018

IoT Intern

Hyderabad

- Worked on the IoT platform including Arduino UNO and esp8266, along with firebase database to build system
 - · Collaborated with team members for researching the Garbage system.
 - · Assisted Team Lead in Hardware connections and simplified the process of Hardware process.

Suniva Notes Pvt Ltd

Aug 2021 - Aug 2021

Patna

Content Intern
- Worked on 10th and 12th Biology Content

• Wrote content on Heredity and Evolution in about approx. 2000 words.

Projects

Major

RISC-V RV32I Processor RTL Design

Xilinx Vivado Ide

- Researched thoroughly about RISC-V; their connections, various blocks, and their working structures.
- Tried basic and simplified coding style of the Verilog for maximum understanding.
- Used basic blocks and their interconnection for simplified and managed structure of the processor.

Minor Projects

- RTL design of I2C protocol (Verilog HDL)
- Simple calculator application (.exe) (python3)
- Image Compressor cum converter app (.exe) (Python3) and (CSS)
- Designed an application to Predict the house prices near future (ML) and (Python3)

Education

Birla Institute of Technology, Mesra

Bachelor of Engineering in Electronics and Communication

Jul 2017 - Jun 2021 CGPA - 6.98/10.0

R.Lal Intermediate College, Alinagar

Jun 2015 - May 2017

Intermediate

Score - 63%

D.A.V. Public School, Nalanda

May 2014

Matriculation

CGPA - 8.8/10.0

Leadership / Extracurricular

- Runner up in college art Fest.
- Runner up in Fashion modelling in Anwesha IIT Patna Fest.
- Art is being published in college annual magazine.