**CURRICULUM VITAE**



Dr. D.R.V.A.SHARATH KUMAR Mobile: 9985511940 Email:acharyasharath79@gmail.com



1. Presently working as a Professor and HOD in ECE Dept. of Malla Reddy Institute of Technology, July 2019 to till the date.
2. Research Project proposal is submitted to SERB (Science and Engineering Research Board) under EMRF and waiting for the approval.
3. Previously Worked as a Principal in Younis Sultan College of Engineering, HYD under JNTUH.
4. Previously Ratified Faculty in ECE department of St. Martins Engineering College
5. Previously Ratified Faculty in ECE Dept of Geethanjali College of Engg & Tech, Keesara, HYD under JNTUH.
6. Appointed as an Enforcement officer for EAMCET 2013 at WARANGAL.
7. Editorial Board member for the International Journal IJSRCSAMS.
8. Expert in NBA, NAAC, Autonomous, NIRF and other Accreditations work and Evaluation.
9. Handled AICTE, JNTUH, NBA, NAAC, UGC Autonomous works, NIRF and TASK FORCE works successfully.
10. Good in provision of Outcome Based Education.

**Responsibilities handled as a Principal and Professor** :

Presently all Academics and Administrative works like:

1 Responsible for the institute management with 1000 students and more than 250 faculty members & 30 Non Teaching staff for academic, examinations, paper correction, placement and industry interface functions, recruitment of faculty/other staff.

1. Managing the interfaces with national authorities (MHRD/UGC/AICTE), University /professional bodies, student activity centers, faculty and student activity forums and other activities like administration, finance, discipline, social service, help centers for scholarships/fees reimbursements, financial support to the needy, sports center etc.

|  |  |
| --- | --- |
| 3 | Created the required environment in enabling the students for getting exposed to |
|  | design oriented effective teaching. |
| 4 | Monitoring the responsibilities of the below mentioned members of that posts. |

1. Developed other cultural activities and state of art laboratories.
2. I designed & developed with the help of faculty members the COURSE FILE and SUBJECT FILE structures, which are necessary for the faculty members to upgrade Faculty subject knowledge, by which student get the good concepts not only as per the curriculum, students get the knowledge as per the industrial requirements, as per the Higher qualification requirements in INDIA, and in the ABROAD
3. Under my PRINCIPAL ship two CAMPUS drives were conducted even in this recession period.
4. Appointed as a member of BOARD OF STUDIES, Department of ECE, Malla Reddy College of Engineering and Technology from the Academic year 2015-16.
5. Appointed as a member of Department Academic Committee, Department of ECE, Malla Reddy College of Engineering and Technology from the Academic year 2015-16.

**Research Work:**

1. In the National and International Conferences Eight (8) papers are presented.
2. In the international Journals twenty one (21) papers are published.
3. In the month of July 2016 Research Project Proposal is submitted to DST under EMRF.

1. In the month of December 2016 Research Project Proposal is submitted to DST under EMRF.
2. Patent is filed and it is published in Office Journal of Patent Office on “Compact Multi functional Smart Laptop”.
3. Patent is filed and it is published in Office Journal of Patent Office on “Smart Domestic Cleaning Gadget”

**EDUCATIONAL QUALIFICATIONS:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **COURSE** | **INSTITUTION** | **BOARD /** | **YEAR OF** | **GRADE** |  |
|  | **UNIVERSITY** | **COMPLETION** |  |
|  |  |  |  |
|  | University College | Andhra | March 2013 | Awarded |  |
| Ph.D | Of Engineering | University |  |  |
|  |  |  |
|  |  |  |  |  |  |
| ME | PDA College Of |  |  |  |  |
| Engineering, | VTU | Aug 2005 | 82.5% |  |
| (ECE) |  |
| Gulburga |  |  |  |  |
|  |  |  |  |  |
|  | S.L.N College of |  |  |  |  |
| B.E (E&C) | Engineering , | VTU | Sept 2002 | 72% |  |
|  | Raichur |  |  |  |  |
| Polytechnic | V.K.R & V.N.B | Technical Board |  |  |  |
| Polytechnic | April 1998 | 53% |  |
| (E&C) | of institution. AP |  |
| College, Gudivada |  |  |  |
|  | Singareni Colliries | Board Of |  |  |  |
| S.S.C | Boys High School, | Secondary | March 1994 | 60% |  |
|  | Kothagudem | Education, AP |  |  |  |

**Software & Hardware Skills:**

C – Language , 8085 & 8086 in Microprocessor, VLSI , Power Electronics ,VHDL, Digital Design, Verilog, Embedeed systems.

**Detailed Work Experience:**

1 Worked as a Assistant Professor for AMINA college of Engg & Tech, HYD from June2002 to May2005.

2 Worked as a Professor and HOD for Geethanjali college of Engg & Tech, HYD from June-2005 to July 2012.

1. Worked as a Principal & Professor for The Younis Sultan College of Engineering, Hyderabad from July 2012 to July 2013.
2. Worked as a Professor for Malla Reddy College of Engineering and Technology,

Hyderabad from July 2013 to June 2016

1. Worked as a HOD and Professor for St. Martins Engineering College, Hyderabad from June 2016 to May 2019.
2. Working as a HOD and Professor for Malla Reddy Institute of Technology, Hyderabad from June 2019 to till now.

**Subjects Handled:**

I. When I was in **Assistant Professor** Post,

* + 1. Electronics Devices and Circuits.
		2. Electronic Circuits Analysis.
		3. Electronics Circuits.
		4. Pulse Digital Circuits.
		5. STLD.
		6. DICA.
		7. LICA.
		8. Micro Processor.
		9. VLSI.
		10. EMI.
		11. DDTV (Verilog ).
		12. Television Engineering.

II. When I was in **Associate Professor** post,

* + 1. Electronics Devices and Circuits.
		2. DICA.
		3. VLSI.
		4. DDTV (Verilog).
		5. Television Engineering.
		6. Low Power VLSI Design (M. Tech).

III. As a **Professor**

* + 1. Low Power VLSI Design (M. Tech).
		2. Wireless LAN PAN.
		3. CMOS Analog Circuit Design
		4. Analog Electronics
		5. Switching Theory And Logic Design
1. Linear Digital Integrated Circuit & Applications

I handled more than **70 projects** for the **B.Tech** students and **30 projects** for **M.Tech** students.

**Projects:**

1. **Electronic Private Automatic Branch Exchange (Done in Diploma)**

**Description:** In this project, we can give the number of interconnection lines through themain connection, i.e., the main connection number is same for all the interconnection lines. We can give the interconnections by the extension numbers.

1. **Electronic Voting machine using 8086 Micro Processor (Done in BE)**

**Description:** With this machine, we can count the number of polled votes in the election.Generally, existing machines are built with 8085 microprocessor. But, this machine is with 8086 microprocessor. In this machine, we can count the votes with the secret code.

**3. Automatic Vehicle Detection (Done in ME).**

The Automatic Vehicle Detection System (AutoVDS) is a system that detects available spaces in a parking lot and relays the information to the Internet where it is available to

interested drivers. AutoVDS will save drivers time and aggravation by informing them of parking availability before they get to the lot, allowing them to pick the best lot if they have a choice. AutoVDS consists of four main components: Digital camera Central processor w/ camera control and detection software Information database The camera and control unit are mounted above the lot - on a building or parking garage for example. The control unit enables the camera to take still pictures of the lot at regular intervals. The images are then run through our detection software, which uses edge detection to determine whether or not each space contains a number of available parking spaces. There are numerous applications for AutoVDS. It will be a great tool not only for drivers commuting to work, school, or the mall, but also for parking lot attendants who are in charge of large lots such as those at sporting events. And in addition to alerting users of available parking spaces, the AutoVDS can be used to inform parking attendants or towing companies of cars that are parked in illegal areas.

**Thesis in Ph.D**: Design for Testability of Asynchronous VLSI Circuits

**Abstract**:

Asynchronous design methodologies are a subject of growing research interest since they appear to offer benefits in low power applications and promise greater design modularity. However, before these advantages can be exploited commercially, it must be shown that asynchronous circuits can be tested effectively in volume production. This thesis presents the results of research into various aspects of the design for testability of asynchronous circuits.

Low power is often achieved by minimizing circuit activity. However, testable designs require high transition probabilities. It is shown that design for testability and design for low power are in direct contact. As a result, the more testable a circuit is, the more power it consumes. The resolution of this contact can be found in the separation of normal operation and test modes. In test mode the circuit activity is increased, dissipating more power. Many asynchronous designs use Muller C-elements in a large variety of applications including both control and data paths. Testable CMOS designs for C-elements are presented which provide for the detection of transistor stuck-at and stuck-open faults.

The scan test technique is used to test stuck-at and delay faults in micro pipelines. This technique is generalized to the design for testability of either two-phase or four-phase micro pipelines. An asynchronous built-in self test (BIST) micro pipeline design based on the BILBO technique is presented. The proposed design for the BILBO register allows stuck-at and delay faults to be detected inside the combinational circuits of the micro pipeline. Structural designs for random pattern test ability techniques applicable to asynchronous sequential circuits are described. The proposed random test procedure provides for the detection of all single stuck-at faults in the control and data paths of the sequential circuit under test, reducing the overall test complexity to the testing of its combinational network. Case studies of testable implementations of some high-level asynchronous functions, including an adder and a block sorter, are analyzed for their testability, performance and area cost. These designs show that, as expected, there is a trade-off to be made between testability and cost. However, satisfactory testability can be achieved for a circuit designed with a small area overhead for test circuitry and little performance degradation

**Research Projects:**

1. A project,” Rural Electrification by Solar Power LED’s” is submitted to Science and Engineering Research Board(SERB) under EMRF and waiting for the Approval.

2. A project,” Flash Interface Subsystem for SSD Controller Architecture” is submitted to Science and Engineering Research Board(SERB) under EMRF and waiting for the Approval.

**National / International Conferences Attended:**

1. **D.R.V.A.Sharath Kumar, Y.Nagalakshmi and G.Sahithi**, presented the paperin the **International Conference** on “**Asynchronous techniques in Nano** **technology”** at **Sreenidhi Institute of Technology and Science**, Hyderabad onJanuary 2012.
2. **D.R.V.A.Sharath Kumar, A.Srinivas**, presented the paper in the **National Conference** on **“Low power VLSI techniques”** at **Geethanjali College of Engineering and Technology,** Hyderabad on February 2012.
3. **D.R.V.A.Sharath Kumar, J.Nagaeshwara Reddy** presented the paper in the **International Conference** on **“Communications, Signal Processing Computing and Information Technologies”** at **Malla Reddy College of Engineering and Technology,** Hyderabad on December 2014 with ISBN of
4. **D.R.V.A.Sharath Kumar, J.Nagaeshwara Reddy** presented the paper in the **National Conference** on **“Developments, Advances & Trends in Engineering Sciences”** at **CMR Engineering College,** Hyderabad on January 2015.
5. **D.R.V.A.Sharath Kumar** presented the paper in the **International Conference** on **“Signal Processing, Communications and System Design”** at **MRECW** **Engineering College,** Hyderabad on July 2015.
6. **D.R.V.A.Sharath Kumar** presented the paper in the **International Conference** on **Communications, Signal Processing, Computing and Information**

**Technologies(ICCSPCIT- 2015) with the topic “Design Of High Speed Standard Gate With Sub Threshold Dual Mode Logic using gpd 45 nm”** at **Malla Reddy College of Engineering and Technology,** Hyderabad on December 2015 withISBN of **978-93-83038-27-5**

1. **D.R.V.A.Sharath Kumar** presented the paper in the **International Conference** on **“Signal Processing, Communications and System Design”** at **Malla Reddy** **Engineering College for Women,** Hyderabad on August 2016.
2. **D.R.V.A.Sharath Kumar** presented the paper in the **International Conference** on **“QR Pattern Driven Hardware Obfuscation Using High Level**

**Transformations ”** at **Akshaya College of Engineering and Technology,** Coimbatore on September 2018.

**National/International Journals Published:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Publications** | **Journal/** | **Title of the paper** | **ISSN/** | **Vol No.** | **Month and** |  |
| **Type** | **Conferenc** |  | **ISBN No.** | **and ISSN** | **Year** |  |
|  | **E** |  |  |  |  |  |
|  | **Name** |  |  |  |  |  |
| International | **IJSRCSAM** | Advanced Image Restoration | 2319 - 1953 | Vol 2 and | Nov 2013 |  |
| Journal | S | For Headway Video Recorders | Issue 6 |  |  |
|  |  |  |
| International | IJRCEE | Migration For Secure Data | 2319-376X | Vol 3 and | March 2014 |  |
| Journal | Acquisition Systems | Issue 2 |  |  |
|  |  |  |  |
| International |  | A Proposed Technique Or |  | Vol 4 and | April 2014 |  |
| IJETAE | Migration To IPV6 For A | 2250-2459 | Issue 4 |  |  |
| Journal |  |  |
|  | Secure SCADA Architecture |  |  |  |  |
|  |  |  |  |  |  |
|  |  | Design Of Multiplier And |  | Vol 2 and | Sep 2014 |  |
| International | IJRASET | Divider Using Reversible Logic | 2321-9653 | Issue 9 |  |  |
| Journal | Gates With Vedic |  |  |  |
|  |  |  |  |  |
|  |  | Mathematical Approach |  |  |  |  |
|  |  | Enhancing Communication |  | Vol 4 and | Sep 2014 |  |
| International | IJESR | Through Multi Users Ofdm | 2277 - 2685 | Issue 9 |  |  |
| Journal | System Efficiencies By |  |  |  |
|  |  |  |  |  |
|  |  | Modulation Implementation |  |  |  |  |
| International |  | Design And Realization Of |  | Vol 1 and | Nov 2014 |  |
| IJERM | Look Up Table, FIR Digital | 2349 - 2058 | Issue 8 |  |  |
| Journal |  |  |
|  | Filter |  |  |  |  |
|  |  |  |  |  |  |
| International |  | Low Complexity Out Of Order |  |  | Jan 2015 |  |
| IJERA | Issue Logic Using Static | 2248 - 9622 |  |  |  |
| Journal |  |  |  |
|  | Circuits |  |  |  |  |
|  |  |  |  |  |  |
| International | IJCCS | Dual Mode Logic Based On | 2277 - 6699 | Vol 4 and | Feb 2015 |  |
| Journal | Sub-Threshold | Issue 1 |  |  |
|  |  |  |  |
|  |  | A 350-MS/S Continuous-Time |  | Vol 3 and | April 2015 |  |
|  |  | Delta–Sigma Modulator With |  | Issue 9 |  |  |
| International | IJRAET | A Digitally Assisted Binary- | 2347 - 2812 |  |  |  |
| Journal | DAC And A 5-Bits Two-Step- |  |  |  |
|  |  |  |  |  |
|  |  | ADC Quantize In 130-Nm |  |  |  |  |
|  |  | CMOS |  |  |  |  |
| International | IJEERT | Compact Implementation Of | 2349 – | Vol 3 and | July 2015 |  |
| Journal | SHA 3 -1024 On FPGA | 4409(4395) | Issue 7 |  |  |
|  |  |  |
|  |  | A Novel Optic Disc |  | Vol 2 and | July 2015 |  |
| International | IJMETMR | Segmentation In Retinal Images | 2348 - 4845 | Issue 7 |  |  |
| Journal | By Using Marcov Random |  |  |  |
|  |  |  |  |  |
|  |  | Field |  |  |  |  |
|  |  | Implementation Of Binary |  | Vol 4 and | Dec 2015 |  |
| International | IJCCS | DAC And two Step ADC | 2277 - 6699 | Issue 2 |  |  |
| Journal | Quantizer For CTDS Using |  |  |  |
|  |  |  |  |  |
|  |  | GPDK 45nm |  |  |  |  |
| International | IJCCS | Design Of High Speed | 2277 - 6699 | Vol 4 and | Dec 2015 |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Journal |  | Standard Gate With Sub |  | Issue 2 |  |  |
|  |  | Threshold Dual Mode Logic |  |  |  |  |
|  |  | Using GPDK 45nm |  |  |  |  |
|  |  |  |  |  | April 2017 |  |
|  |  | Input Driven Dynamically |  | 2017(marc |  |  |
|  |  |  | h and |  |  |
| International |  | Reconfigurable Fixed Width |  |  |  |
| **RJPBCS** | 0975-8585 | april)& |  |  |
| Journal | Multiplier For Low Power DSP |  |  |
|  |  | Volume |  |  |
|  |  | Applications” |  |  |  |
|  |  |  | 8,issue2, |  |  |
|  |  |  |  |  |  |
|  |  |  |  | Paper 114 |  |  |
| International | IJTSRD | Rural Electrification By Solar | 2456-6470 | Vol 1 and | May 2017 |  |
| Journal | Power LED’s | Issue 5 |  |  |
|  |  |  |  |
| International |  | Implementation Of Four |  | Vol 4 and | Nov 2017 |  |
| IJMETMR | Wheeler Parking Management | 2348-4845 | Issue 11 |  |  |
| Journal |  |  |
|  | System |  |  |  |  |
|  |  |  |  |  |  |
| International |  | The Possibility Of Multipart |  | Vol 4 and | Jan 2018 |  |
| IJTIMES | Driven Flip Flop Integration | 2455-2585 | Issue 1 |  |  |
| Journal |  |  |
|  | With Clock Fusion” |  |  |  |  |
|  |  |  |  |  |  |
| International | **IJSRCSAM** | “Modeling And Simulation Of | 2319-1953 | Vol 6 Issue | Nov 2017 |  |
| Journal | **S** | RF MEMS Switches” | 6 |  |  |
|  |  |  |
|  |  | Implementation of Fault |  | Vol 6 and | Dec 2018 |  |
|  |  |  | Issue 4 |  |  |
| International |  | Identification System in the |  |  |  |
| **IJRECE** | 2393-9028 | Version 3 |  |  |
| Journal | wind turbine using CAN |  |  |
|  |  | Paper id |  |  |
|  |  | protocol |  |  |  |
|  |  |  | f645 |  |  |
|  |  |  |  |  |  |
|  |  |  |  | Vol 8 and | July 2019 |  |
| International |  | Hardware obfuscation driven |  | Issue 1.3 |  |  |
| **IJATCSE** | by QR pattern using high level | 2278-3091 | (Special |  |  |
| Journal |  |  |
|  | transformations |  | Issue) |  |  |
|  |  |  |  |  |
|  |  |  |  | Article 8 |  |  |
|  |  |  |  | Vol 10 and | Feb 2020 |  |
| International | **IJECE** | A Test architecture design for | 2088-8708 | Issue 1 Part |  |  |
| Journal | SOC’s using Atam method | 2 paper ID |  |  |
|  |  |  |  |
|  |  |  |  | 719 |  |  |
|  |  |  |  | Vol 23 and | Dec 2019 |  |
| International | **IJPE** | Three tire security system for | 1475-7192 | Issue 1 |  |  |
| Journal | Electronic Voting Machine | Paper ID: |  |  |
|  |  |  |  |
|  |  |  |  | 449 |  |  |
|  |  | Information encryption |  | Vol 23 and | Dec 2019 |  |
| International |  |  | Issue 1 |  |  |
| **IJPE** | methods to reduce networks on | 1475-7992 |  |  |
| Journal | Paper ID: |  |  |
|  | chip energy efficiency |  |  |  |
|  |  |  | 455 |  |  |
|  |  |  |  |  |  |

**Workshop Attended/Participated:**

1. Workshop participated on **“Rough Sets**” at **Malla Reddy College of** **Engineering and Technology, Hyderabad** from 02-12-2013 to 04-12-2013

conducted by Malla Reddy College of Engineering and Technology.

1. Workshop participated on **“Signals and Systems” at Malla Reddy College of**

**Engineering and Technology, Hyderabad** from 02-01-2014 to 12-01-2014conducted by **IIT KHARAGPUR.**

1. Workshop attended on **“Design of Algorithims” at Malla Reddy College of**

**Engineering and Technology, Hyderabad** from 25-05-2015 to 31-06-2015conducted by **IIT KHARAGPUR.**

1. Workshop attended on **“Embedded Linux on ZYNQ –** **7000 SOC Using**

**VIVADO ” at Malla Reddy College of Engineering and Technology,**

**Hyderabad** on 25-09-2015 conducted by **COREL Technologies in Association with DIGILENT and XILINX.**

1. Workshop attended on **“Ultra Low Power Micro Controllers for Analog and**

**Digital Design using TI tools” at St. Martin’s Engineering College,**

**Hyderabad** on 19-01-2017 conducted by **Texas Instruments.**

1. Webinar attended on **“Online Teaching Learning and Online Assessment** **Platform”** on 29-04-2020 conducted by **inpods.**
2. Webinar attended on **“Programming for every body:Python”** on 29-04-2020 conducted by **Skillzcafe(Charles severance).**
3. Webinar attended on **“Expectation of Industry from Students”** on 01-05-2020 conducted by **ieee photonics students chapter Mangalam College of**

**Engineering, Kottayam .**

1. Webinar attended on **“Cutting Edge Technologies in Electronics and Communication Engineering”** from 14-05-2020 to 16-05-2020 conducted by **G.Pullaiah Reddy College of Engineering and Technology, Kurnool.**
2. FDP attended on **“Recent Communication Tools and its Applications”** from 19-05-2020 to 23-05- 2020 conducted by **Department of ECE, St.Martin’s Engineering College, Hyderabad .**
3. Technical Quiz attended on **“Electrical Engineering”** from 29-05-2020 to 01-05-2020conducted by **MLR Institute of Technology, Hyderabad .**
4. Webinar attended on **“Exponential growth of emerging area”** on 30-05-2020 conducted by Department of Electronics and Communication Engineering, **Saveetha Engineering College, Chennai.**
5. Webinar attended on **“Learn basic android app development techniques in an Hour"** on 31-05-2020 conducted by **Department of Electronics and Communication Engineering, Saveetha Engineering College, Chennai.**

**International / National Conferences/Technical Symposiums Organized:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.** | **Title of the Conference** | **Period** | **Place** |
| **No** |  |  |  |
| 1. | National Conference on “Present | 09-09-2005 - | Amina Institute of Engineering |
|  | Trends in the VLSI technology”. | -- 10-09- | and Technology Hyderabad. |
|  |  | 2005 |  |
| 2. | National Conference on “Industrial | 19-12-2008 - | Geethanjali College of |
|  | Digital systems”. | -- 20-12- | Engineering and Technology |
|  |  | 2008 | Hyderabad. |
| 3. | National Conference on “Emerging | 12-08-2010 - | Geethanjali College of |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  | Trends in the Embedded Systems”. | -- 13-08- |  | Engineering and Technology |
|  |  |  |  |  | 2010 |  | Hyderabad. |
|  | 4. |  | National Conference on “Wireless | 09-03-2012 - |  | Geethanjali College of |
|  |  |  | Communication”. | -- 10-03- |  | Engineering and Technology |
|  |  |  |  |  | 2012 |  | Hyderabad. |
|  | 5 |  | National Level Technical | 26-09-2014 - |  | Malla Reddy College of |
|  |  |  | Symposium | -- 27-09- |  | Engineering and Technology |
|  |  |  |  |  | 2014 |  |  |
|  | **WORK-SHOPS ORGANIZED:** |  |  |  |  |
|  |  |  |  |  |  |  |
|  | **S.** |  | **Title of the Short Term Course** | **Period** |  | **Place** |
|  | **No** |  |  |  |  |  |  |
|  | 01. |  | Two day workshop on Image | 10-06-2005 -- |  | Amina Institute of Engineering |
|  |  |  | Processing | - 11-06-2005 |  | and Technology Hyderabad. |
|  | 02. |  | Two day workshop on Data | 19-06-2009 -- |  | Geethanjali College of |
|  |  |  | Communications | - 20-06-2009 |  | Engineering and Technology |
|  |  |  |  |  |  |  | Hyderabad. |
|  | 03. |  | Two day workshop on Micro | 15-06-2012 -- |  | Geethanjali College of |
|  |  |  | Processor and Micro Controllers | - 16-06-2012 |  | Engineering and Technology |
|  |  |  |  |  |  |  | Hyderabad. |
|  | 04 |  | Three day workshop on Ultra Low | 19-01-2017 -- |  | St.Martin’s Engineering |
|  |  |  | Power Micro Controllers for Analog | - 21-01-2017 |  | College,Hyderabad. |
|  |  |  | and Digital Design using TI tools |  |  |  |

**Invited Guest Lectures / Seminars:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.** | **Name of the topic** | **Period** | **Organization** |
| **No** |  |  |  |
| 1. | Asynchronous Techniques | 22-12-2011 | Amina Institute of Engineering and |
|  | in VLSI |  | Technology |
| 2. | Digital Logic Systems | 24-2-2012 | TKR College of Engineering and |
|  |  |  | Technology |
| 3. | VLSI Technology | 16-8-2012 | Avanthi College of Engineering and |
|  |  |  | Technology |
| 4. | Design For Testability | 15-03-2013 | TKR College of Engineering and |
|  |  |  | Technology |
| 5. | Low Power VLSI | 24-10-2013 | The Younis Sultan College of |
|  | Technology |  | Engineering |

**Invited Judge:**

|  |  |  |  |
| --- | --- | --- | --- |
| **S. No** | **National/International** | **Period** | **Organization** |
|  | **conference/Technical** |  |  |
|  | **Symposium** |  |  |
| 1. | National Technical | 17-09-2010 & | Amina Institute of |
|  | Symposium | 18-09-2010 | Engineering and |
|  |  |  | Technology |
| 2. | National Conference | 12-08-2011 & | Avanthi College of |
|  |  | 13-08-2011 | Engineering and |
|  |  |  | Technology |
| 3. | National Conference | 17-02-2012 & | The Younis Sultan College |
|  |  | 18-02-2012 | of Engineering |
| 4. | National Conference | 20-09-2013 & | BVRIT College of |
|  |  | 21-09-2013 | Engineering and |
|  |  |  | Technology |
| 5. | National Conference | 31-01-2014 & | Malla Reddy Engineering |
|  |  | 01-02-2014 | College for Women |
| 6. | National Conference | 07-03-2014 & | Malla Reddy Institute of |
|  |  | 08-03-2014 | Technology |
| 7 | National Conference | 09-08-2014 | Malla Reddy Engineering |
|  |  |  | College for Women |
| 8. | National Conference | 30-01-2015 | Malla Reddy Engineering |
|  |  |  | College for Women |

**Contributions for the growth of the Departments (ECE) at College level:**

1. Governing body Member, Geethanjali College of Engineering and Technology, Cheeryal (v), R.R.Dist. Andhra Pradesh.
2. Department was accredited by NBA of AICTE thrice during my tenure as NBA Department Coordinator.
3. Departmental In-charge for World Bank Scheme Under TEQIP
4. New and Advanced Laboratories Development
5. Preparation of laboratory manuals and course files
6. Well versed with courses of both ECE and CSE at UG and PG level which are Advantages to the institution.

1. Conducted National level/International level Conferences/Workshops.
2. Invited Guest Lectures/Seminar Talks for the Departmental/College growth.
3. Board of Studies member, Malla Reddy College of Engineering and Technology.
4. Department Academic Committee member, Malla Reddy College of Engineering and Technology.

**Responsibilities handling/handled till now**

1. Coordinator for Discipline and Grievance committee.
2. Coordinator for Personality Development Program.
3. Coordinator for Transport.
4. Coordinator for Class-In charges.
5. Coordinator for Sports.
6. Coordinator for Projects.
7. Coordinator for Industrial tours.
8. Coordinator for Industrial visits.
9. Coordinator for Guest lectures.
10. Coordinator for Mentor diaries.
11. Coordinator for the College Level Placement Training
12. College level Coordinator NBA Works,

Under my guidance 30 projects were successfully completed by the M.Tech students till now and 75 Mini and Major Projects were successfully completed by the B.Tech students.

**Personal Profile:**

Name:

Father’s Name:

Date of Birth:

Gender:

Marital Status:

Nationality:

Languages Known:

Mother Tongue:

D.R.V.A. Sharath Kumar

D. Krishnama Charyulu

15th August 1979

Male

Married

Indian

Telugu, Hindi, English & Kannada

Telugu

Date:

Place:

(Dr.D.R.V.A.SHARATH KUMAR)