Ujjwal Leyangi

Email: Ujjwalleyangi123@gmail.com

ACADEMIC DETAILS

Motilal Nehru National Institute of Technology, Allahabad- India **CPI-8.05**
B. Tech in Electronics and Communication Engineering (2018)
Delhi Public School, Ranchi- India **Percentage- 88.60%**
All India Senior School Certificate Examination (2014)
St. Charles School, Ranchi- India **Percentage- 93.85%**
Indian Certificate for Secondary School Examination (2012)

TECHNICAL SKILL AND INTEREST

Area of interest: Digital Design, Embedded Systems
Language used: C, C#, Verilog HDL
IDEs used: Xilinx ISE
Relevant Courses: VLSI Design and embedded systems (8051 microcontroller)

EXPERIENCE

Worked as a Graduate Engineer Trainee in Fire Detection Product Development at Johnson Controls India Engineering. **Sept'18 – Sept'19**

Won award for Best executed program FY19 by Johnson Controls India Engineering for NG Designer Release A.

Worked on the Project NG Consys which involved brief usage of the following applications: Jira, Visual Studio, Agile Software Development.

PROJECTS / INTERNSHIP / TRAINING

1. **Summer Training of Verilog and Embedded Systems at MNNIT Allahabad June'16 – July'16**
   Basic Output :-
   - **Designed a 16bit ALU using Verilog HDL**
     - Designed and implemented 16 bit ALU using Verilog HDL
     - Implemented addition, subtraction, multiplication.
     - Exposure: Digital Design, Verilog HDL
   - **Implemented light to frequency module interfacing**
     - Interfaced TSL 230 light to frequency converter
     - Exposure: 8051 microcontroller (timers and interrupts)
2. **Project on Wireless morse code messenger using Atmega 32 microcontroller** **Nov'16 – Nov'16**
   - Morse code unit was taken through a push button and was encoded and wirelessly transmitted.
   - At receiver end it was decoded and was displayed on 16x2 lcd display.
   - RF module operating at 434 MHz was used for wireless communication.
   - Encoder and Decoder IC's HT 12E and HT 12D was used for encoding and decoding the data respectively.
3. **Summer Internship at Aone Solution Private Limited.** **May'17 – June'17**
   - Worked as a counsellor and learnt ways to interact with clients.
4. **Design of low power and high speed one bit hybrid full adder.** **Oct'17- Nov'17**
   - Mentor Graphics was used to design the circuit diagram of a one bit full adder.
   - Circuit was tested for power and delay using Mentor Graphics tools.
5. **Design of power and area efficient approximate multiplier.** **March'18-April'18**
   - Verilog HDL was used to implement approximate multiplier.
   - Power and Area were calculated using Synopsys.

ACHIEVEMENTS

Runner up at Automax event at MNNIT Allahabad in 2014.

Runner up at E-plan event of Entrepreneur summit at MNNIT Allahabad in 2018.

HOBBIES

Writing short stories, listening music.

PERSONAL DETAILS

Date of Birth: 30th August 1996 Linkedin: https://www.linkedin.com/in/ujjwal-leyangi-40427412a/
Contact: 7764825448 Skype:Ujjwalleyangi123@outlook.com